Claims

What is claimed is:

1. A method of testing a memory die, comprising:

allowing said memory die to be placed in a location outside of a production facility of said die;

testing said memory die while said die is in said location; and

storing a partial memory cell address on said die as a result of said testing act, wherein said address corresponds to a memory cell having failed said testing act.

2. The method in claim 1, wherein said testing act comprises testing said die while said die is part of an electronic system.

3. The method in claim 2, wherein said testing act comprises testing said die while said electronic system is in a power management mode.

4. The method in claim 2, wherein said testing act comprises testing said die while said die is part of a computer system.

5. The method in claim 2, wherein said testing act comprises testing said die while said die is part of a telephone system.

6. The method in claim 5, wherein said testing act comprises testing said die while said die is part of a cellular telephone system.

7. A method of repairing a memory die, comprising:

reconfiguring an electrical communication path within said memory die subsequent to:

removing said memory die from a production facility for said die, and

incorporating said die as part of an electronic system;

retaining said die as part of as part of said electronic system during said reconfiguring act; and

indefinitely retaining said die as part of as part of said electronic system after said reconfiguring act.

8. The method in claim 7, wherein said reconfiguring act comprises programming a programmable element.

9. The method in claim 8, further comprising transmitting a result of said reconfiguring act to an output device of said electronic system.

10. A method of processing a plurality of memory circuits, comprising:

incorporating said plurality of memory circuits into an electronic system, said system having a primary function other than test or repair of said plurality of memory circuits; and

transmitting a signal in parallel to said plurality of memory circuits, said signal relating to a selection consisting of simultaneously testing said plurality of memory circuits and simultaneously repairing said plurality of memory circuits, said transmitting act occurring while said plurality of memory circuits are incorporated into said electronic system.

11. The method in claim 10, wherein said transmitting act comprises transmitting a signal in parallel to a plurality of die, wherein each die of said plurality of die comprises at least one memory circuit.

12. The method in claim 11, wherein said transmitting act comprises transmitting a signal to a module comprising said plurality of die.

13. A method of processing a memory die, comprising:

incorporating said memory die into an electronic system for an indefinite amount of time; and

physically rerouting an electrical communication path of said die while said die is part of said electronic system.

14. The method in claim 13, wherein:

said incorporating act comprises incorporating said die into an electronic system comprising control circuitry and an input device coupled to said control circuitry; and

said rerouting act comprises rerouting in response to said control circuitry receiving a signal from said input device.

15. The method in claim 13, wherein said

said incorporating act comprises incorporating said die into an electronic system comprising control circuitry and at least one input device coupled to said control circuitry; and

said rerouting act comprises rerouting in response to said control circuitry receiving no signal from any input device for a span of time.

16. The method in claim 13, wherein:

said incorporating act comprises incorporating said die into an electronic system comprising control circuitry; and

said rerouting act comprises initiating rerouting with said control circuitry.

17. The method in claim 13, further comprising adding rerouting software to said electronic system before said rerouting act.

18. The method in claim 17, wherein said act of adding rerouting software comprises downloading said software from an internet site into said electronic system.

19. The method in claim 18, wherein said downloading act comprises downloading a BIOS update comprising at least one instruction concerning programming at least one element on said memory die.

20. The method in claim 19, wherein said act of rerouting comprises transmitting a signal to said memory die from another component of said electronic system, wherein said signal is configured to program at least one element on said memory die.

21. The method in claim 20, wherein said act of rerouting comprises programming at least one element on said memory die.

22. The method in claim 21, wherein said act of rerouting comprises allowing said memory die access to a voltage sufficient to program at least one element on said memory die.

23. A method of operating an electronic system including memory, comprising:

initiating a power management mode of said electronic system;

testing said memory while said electronic system is in said power management mode; and

storing at most a partial result of said testing act within said electronic system.

24. The method in claim 23, further comprising downloading instructions into said electronic system while said electronic system is in said power management mode.

25. The method in claim 24, further comprising physically repairing said memory while said electronic system is in said power management mode.

26. A method of operating memory, comprising:

indefinitely incorporating said memory into a computer system; and

initiating a memory test while said memory is part of said computer system,

wherein said memory test comprises:

writing a data pattern from a microprocessor of said computer system to said memory,

continuing to transmit said data pattern from said microprocessor to said memory during a read mode of said memory,

comparing data stored on said memory as a result of said writing act with said data pattern transmitted during said read mode, and

storing less than a full address from said memory as a result of said memory test.

27. The method in claim 26, wherein said storing act occurs in a storage device sharing a common substrate with said memory.

28. The method in claim 26, wherein said initiating act comprises receiving a signal from an input device of said computer system.

29. The method in claim 26, wherein said initiating act comprises transmitting a signal from said microprocessor.

30. The method in claim 26, further comprising transmitting a signal to an output device of said computer system, wherein said transmitting act occurs in response to said result.

31. The method in claim 26, further comprising obtaining memory repair instructions, wherein said obtaining act occurs in response to said result.

32. The method in claim 26, further comprising supplying a voltage to said memory in response to said result, wherein said voltage has a magnitude sufficient to affect any unprogrammed element on said memory.

33. A method of preparing a memory circuit for an alteration of its configuration, comprising:

providing a plurality of memory elements which define a plurality of redundant planes, wherein each memory element of said plurality of memory elements has an address;

incorporating said memory circuit into an electronic system for an indefinite amount of time; and

searching for particular memory elements from said plurality of memory elements, wherein said particular memory elements are isolated from input and output terminals of said memory circuit, wherein said particular memory elements share a partial address, wherein said partial address is relevant to at least two redundant planes, and wherein said searching act occurs subsequent to said incorporating act.

34. The method in claim 33, further comprising storing at most said partial address in a storage device.

35. The method in claim 34, wherein said storing act comprises storing at most said partial address in a storage device, wherein said storage device shares a common support surface with said memory circuit.

36. The method in claim 34, wherein said storing act comprises storing at most said partial address in a storage device, wherein said storage device is configured to hold an amount of data corresponding to at most that of said partial address.

37. A method of in-field programming of an electronic circuit on a chip, comprising:

incorporating said electronic circuit into a computer system for an indefinite period of time;

generating a plurality of signals, an effect of which is configured to program an

element within said circuit, wherein said generating act occurs external to said chip, and wherein said generating act occurs while said electronic circuit is part of said computer system;

altering at least one of said plurality of signals, wherein said altering act occurs external to said chip; and

maintaining said effect despite said altering act, wherein said maintaining act occurs internal to said chip.

38. The method in claim 37, wherein said maintaining act comprises maintaining said effect for a time sufficient to program said element.

39. The method in claim 38, wherein said altering act occurs while said electronic circuit is part of said computer system.

40. The method in claim 39, wherein said maintaining act occurs while said electronic circuit is part of said computer system.

41. An electronic system, comprising:

control circuitry;

at least one input device coupled to said control circuitry;

at least one output device coupled to said control circuitry; and

a memory device coupled to said control circuitry and comprising:

at least one memory cell, and

a register configured to hold less than a full address of at most one memory cell at a time.

42. The electronic system of claim 41, wherein said control circuitry, said at least one input device, said at least one output device, and said memory device define a computer system.

43. The electronic system of claim 41, wherein said control circuitry, said at least one input device, said at least one output device, and said memory device define a telephone system.

44. The electronic system of claim 41, wherein said memory device is part of a package.

45. The electronic system of claim 44, wherein said memory device is part of a single-die package.

46. The electronic system of claim 44, wherein said memory device is part of a multi-chip module.

47. A memory package, comprising:

at least one semiconductor die, each of said at least one semiconductor die comprising:

at least one memory cell, and

a register sized to store less than a full memory cell address; and

passivation material covering at least a portion of each of said at least one semiconductor die.

48. The memory package in claim 47, wherein said at least one semiconductor die comprises a single die; and said package further comprises a lead frame coupled to said single die and extending beyond said passivation material.

49. A memory module, comprising:

a support surface;

a plurality of memory die mounted to said support surface, wherein each die of said plurality includes at least one program element; and

a trace coupled to said support surface and to said plurality of memory die,

wherein said trace is configured to carry signal sufficient to blow any unprogrammed program element on any of said plurality of memory die.

50. The memory module of claim 49, further comprising a conductive contact coupled to said support surface, coupled to said trace, and configured to electrically communicate with an external device.

51. The memory module of claim 49, wherein at least one memory die of said plurality includes a first storage device configured to store data relating to existence of a failed memory cell and at most a part of an address of said failed cell.

52. The memory module of claim 51, wherein at least one memory die of said plurality includes a second storage device configured to store data relating to at most a part of an address of a redundant cell.

53. A motherboard, comprising:

an electrically insulative substrate;

a terminal on said substrate configured to carry a programming voltage; and

a socket coupled to said terminal and configured to receive a memory device.

54. The motherboard in claim 53, further comprising an input/output connection coupled to said terminal.